# New Booster Corrector Magnet

# Power Amplifier Controls

# Draft Specification

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## *General Specification*

We are planning to install 24 new corrector magnet packages into the Booster in the Summer of 2007 and another 24 units in the Summer of 2008. Each of these packages contains 6 magnets, for a total of 288 magnets and associated power amplifiers. The power amplifiers and associated control electronics will be distributed into 6 locations around the Booster Gallery. The power amplifier controls in each of the 6 locations will need to support the functions for 48 power amplifiers. We are requesting a new CAMAC module that would provide the controls and I/O for four independent power amplifiers (or power supplies). The analog and digital I/O and programmable parameters associated with each of the four controlled devices will include the following.

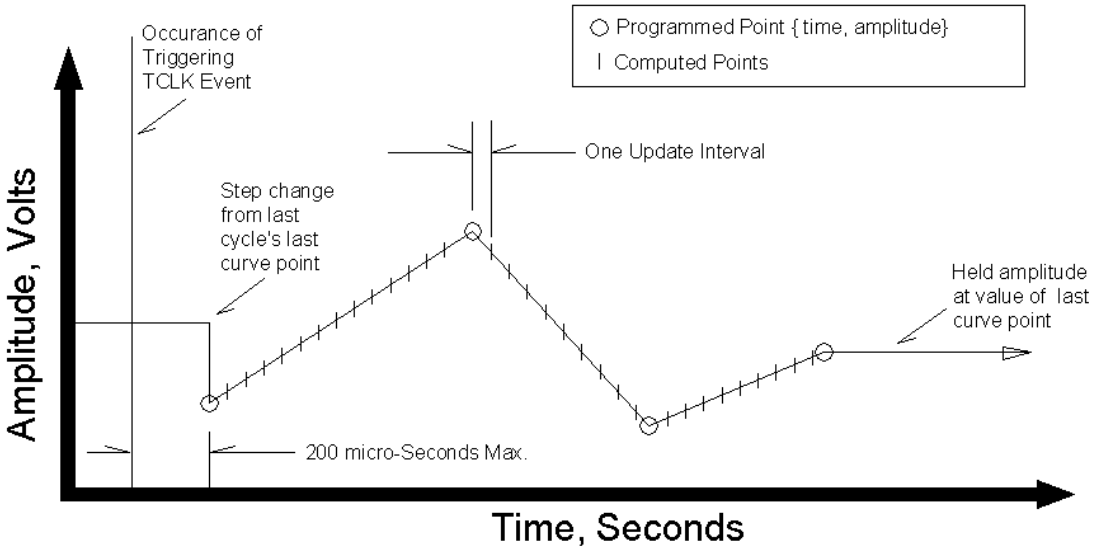
1. Provide ACNET programmable DAC ramp voltage outputs with the following analog parameters.
    a. +/- 10 Volts output into >20K Ohms.
    b. Output should be repeatable to within +/- 0.6 milli-Volts over a 20 degC to 40 degC temperature range.
    c. Output zero offset should be less than 1.0 milli-Volt.
    d. 30 k updates per second or higher (100 k would be useful in other Booster applications).
    e. 16 Bit nominal DAC resolution.
    f. All curve outputs within a single module are expected to start at the same time (+/-200 nano-Seconds).

2. The ramp voltages output from the DAC will have 26 possible programmable "modes" (A thru Z).
    a. There will be 8 programmable TCLK events for each mode that will trigger the playing out of the ramps associated with that mode. This setting applies to all four channels on the module. All four ramps on the module are started simultaneously. Any particular TCLK event will be limited to triggering only one of the 26 modes for a particular controlled device. There are 256 unique TCLK events that the operator may chose from as one of the possible 8 events that trigger one of the possible 26 modes.
    b. For each mode there is a programmable delay that applies to all four channels between the receipt of the TCLK event plus a minimum delay of 100 micro-Seconds and the start of the playing of the ramps. The delay parameter shall have a range from 0 to 100 micro-Seconds and have a resolution of 1.0 micro-Seconds. That is the delay between the receipt of the TCLK event and the start of the ramp will be variable between 100 and 200 micro-Seconds with a resolution of 1.0 micro-Seconds.
    c. For each of the four channels, each mode will have associated with it a particular **ramp curve**, a scalar **scale factor** parameter which will scale the amplitude of the ramp curve, and a curve **bias value** which will offset the curve in amplitude. Both the ramp curve "set of points", the scale factor, and the bias value are set by

the operator for each mode of each channel. How the ramp curves are defined by the operator is defined below.

NOTE: The ability to specify an MDAT variable that also scales the amplitude of the ramp curve may be desirable in application areas other than the Booster. I/O and processing power for this should be available in the new module, but need not be developed for the Booster application. It is recommended that you consult the experts on how MDAT is used in the existing C465 modules.

3. Curves for each mode of each of the four channels on a module will be defined by the operators and users as time-amplitude pairs. Each curve should support 64 of these pairs. Time is a delta-T time span between successive points. The Time coordinate will have a resolution equal to the inverse of the DAC update rate. *However, the minimum delta-T time span between points is limited to 100 micro-Seconds.* The final curves that are played out through the DAC's will be a piecewise linear, point-to-point connection of the time-amplitude pairs. The amplitude of the last defined point will be held until the beginning of the next cycle (see plot below). If it is desired to ramp the output to zero at the end of the cycle the operator must define a final point with amplitude zero.




Note: The most important part of the Booster cycle is the 40 milli-Seconds when the beam may be in the machine. Between the time the beam leaves the machine and when it may possibly be there again, we may want to ramp the amplifiers down to reduce heating and then ramp them back up to be in the neighborhood of where we will likely want to start the amplifiers at for the next cycle. I cannot imagine defining more than 3 points in this region. At 15 Hz cycling of the machine, the period to cover would be 66 milli-Seconds.

4. Provide an analog voltage readback for each controlled device. In the standard application this will be the current monitor output of the power amplifier or switch-mode power supply. The parameters for this digitized input are the following.

a. +/- 10V input.
b. 30 k updates per second.
c. 16 Bit nominal ADC resolution.
d. Zero input offset should be less than 1.0 milli-Volt (3 counts).
e. Readback memory must cover a 40 ms time span (ie at least 1200 points per curve or more).

5. Provide a function to compare the desired current setting determined by the DAC ramp values with the current monitor read back to determine if the power amplifier is sufficiently tracking the desired ramp. The difference between the desired and actual power amplifier current will be compared to an ACNET programmable +/- threshold. A status back to ACNET will indicate whether the current difference magnitude goes outside this window. The status would need to be latched for an appropriate amount of time so that the occurrence of tracking errors would not be missed.

6. For each of the four channels provide an input for a +/- 5 Volt analog voltage that can be summed with the DAC channel outputs via manual jumper or DIP switch settings. A gain of x2 should be provided between this input and the final DAC channel output.

7. Provide four digital outputs (one for each channel) for use as the power amplifier ACNET Enable/Inhibit **and** four digital outputs (one for each channel) for use as the amplifier Fault Resets. The inputs we must interface to are shown in Figure 1 and Figure 2. The Enable and Reset signals will be active low and the driver must be able to sink at least 10 milli-Amps.

8. Four digital logic interlock inputs (one for each channel) should be available on the module to be summed with the remote power amplifier inhibit from ACNET to inhibit the output of power amplifier. These inputs will be derived from temperature threshold comparisons, power amplifier failure indications, door interlocks, flow switches, etc.

9. Provide for read back to ACNET of eight status bits ( TTL at < 10 mA source current) for each power amplifier.

10. The minimum time interval available between the TCLK event that defines the mode to the time the DAC outputs need to be set to their first point is 100 micro-Seconds.

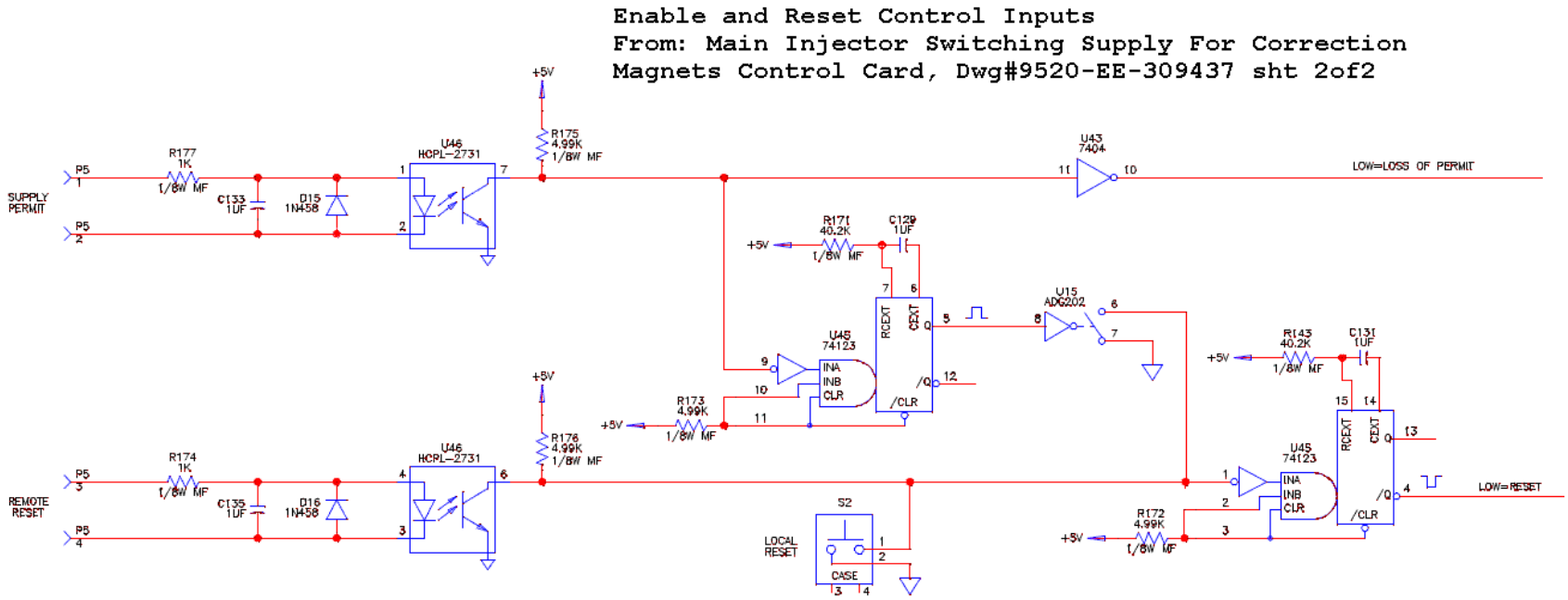

Enable and Reset Control Inputs
From: Main Injector Switching Supply For Correction
Magnets Control Card, Dwg#9520-EE-309437 sht 2of2
SUPPLY PERMIT
REMOTE RESET
LOCAL RESET
LOW=LOSS OF PERMIT
LOW=RESET
+5V
R177 1K 1/8W MF
R174 1K 1/8W MF
C133 1UF
C135 1UF
D15 1N458
D16 1N458
U46 HCPL-2731
R175 4.99K 1/8W MF
R176 4.99K 1/8W MF
R171 40.2K 1/8W MF
R173 4.99K 1/8W MF
R172 4.99K 1/8W MF
R143 40.2K 1/8W MF
C129 1UF
C131 1UF
U43 7404
U15 ADG202
U45 74123
INA
INB
CLR
/CLR
REXT
CEXT
/Q
S2
CASE

Figure 1

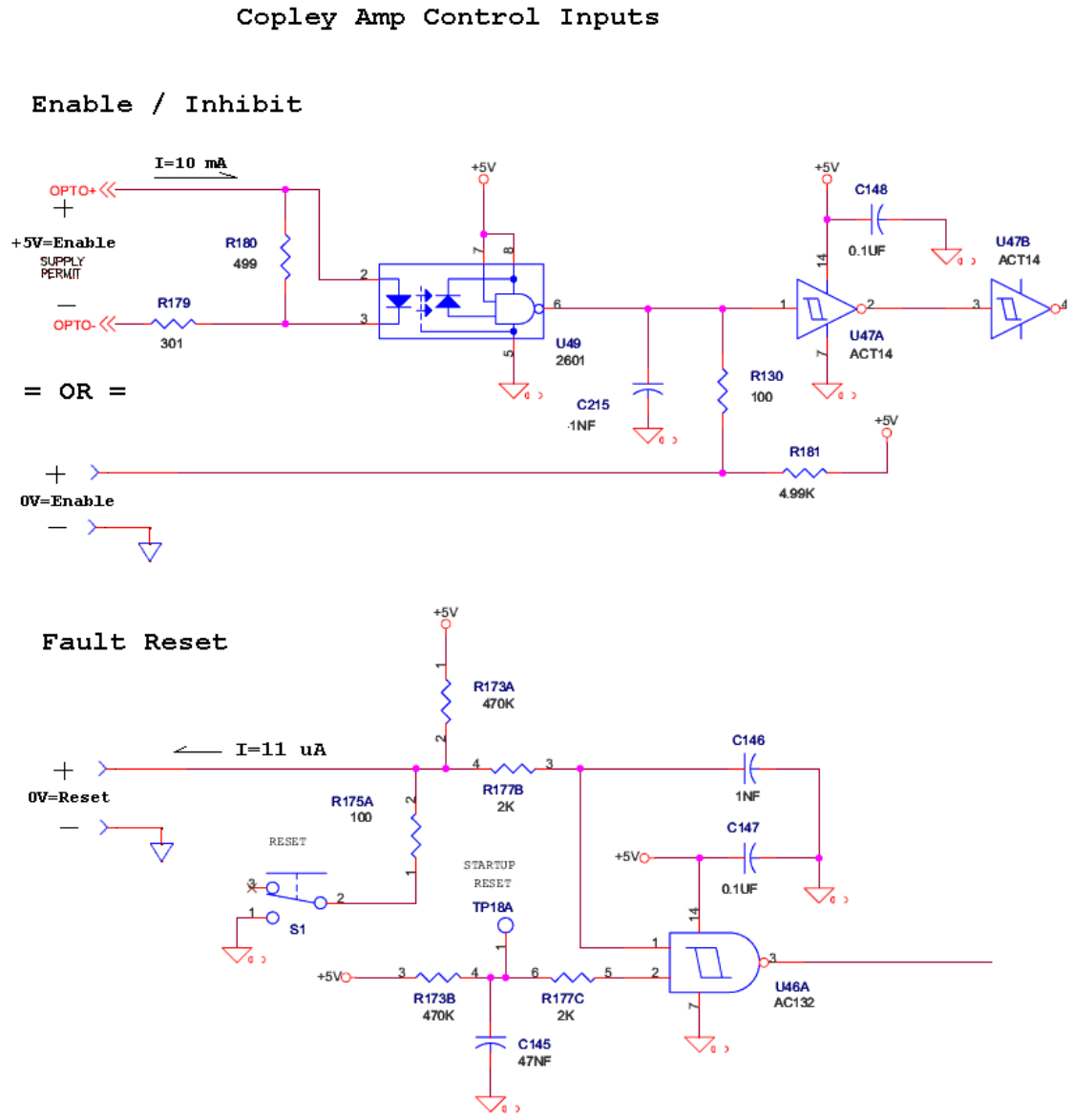

Copley Amp Control Inputs
Enable / Inhibit
I=10 mA
OPTO+
+5V=Enable
SUPPLY PERMIT
OPTO-
R180
499
R179
301
= OR =
0V=Enable
+5V
U49
2601
C215
.1NF
R130
100
C148
0.1UF
U47B
ACT14
U47A
ACT14
R181
4.99K
Fault Reset
I=11 uA
0V=Reset
R173A
470K
R177B
2K
C146
1NF
R175A
100
RESET
S1
STARTUP RESET
TP18A
C147
0.1UF
R173B
470K
R177C
2K
C145
47NF
U46A
AC132

Figure 2.

## APPENDIX A

Preliminary Booster Corrector Controller I/O Proposal – A. Franck – 1/30/06

"A" Board Viking Connector

1L – MDAT Digital Gnd
1R – TCLK Digital Gnd
2L – TCLK Output
2R – TCLK Input
3L – MDAT Output
3R – MDAT Input

4L – TTL Output – Enable Supply 1
4R – TTL Output – Reset Supply 1
5L – TTL Output – Enable Supply 2
5R – TTL Output – Reset Supply 2
6L – Digital Gnd
6R – Digital Gnd
7L – TTL Output – Enable Supply 3
7R – TTL Output – Reset Supply 3
8L – TTL Output – Enable Supply 4
8R – TTL Output – Reset Supply 4

9L – Opto Anode Supply – 5 Volts provided by Supply 1
9R – Status Input 1-1 – (pull low for active state)
10L – Status Input 1-2
10R – Status Input 1-3
11L – Status Input 1-4
11R – Status Input 1-5
12L – Status Input 1-6
12R – Status Input 1-7
13L – Status Input 1-8
13R – Interlock Input 1

14L – Opto Anode Supply – 5 Volts provided by Supply 2
14R – Status Input 2-1 – (pull low for active state)
15L – Status Input 2-2
15R – Status Input 2-3
16L – Status Input 2-4
16R – Status Input 2-5
17L – Status Input 2-6
17R – Status Input 2-7
18L – Status Input 2-8
18R – Interlock Input 2

“B” Board Viking Connector

1L – Analog Reference Output 1
1R – Analog Reference Ground 1
2L – Analog Current Readback 1
2R – Analog Bias Input 1

3L – Analog Reference Output 2
3R – Analog Reference Ground 2
4L – Analog Current Readback 2
4R – Analog Bias Input 2

5L – Analog Reference Output 3
5R – Analog Reference Ground 3
6L – Analog Current Readback 3
6R – Analog Bias Input 3

7L – Analog Reference Output 4
7R – Analog Reference Ground 4
8L – Analog Current Readback 4
8R – Analog Bias Input 4

9L – Opto Anode Supply – 5 Volts provided by Supply 3
9R – Status Input 3-1 – (pull low for active state)
10L – Status Input 3-2
10R – Status Input 3-3
11L – Status Input 3-4
11R – Status Input 3-5
12L – Status Input 3-6
12R – Status Input 3-7
13L – Status Input 3-8
13R – Interlock Input 3

14L – Opto Anode Supply – 5 Volts provided by Supply 4
14R – Status Input 4-1 – (pull low for active state)
15L – Status Input 4-2
15R – Status Input 4-3
16L – Status Input 4-4
16R – Status Input 4-5
17L – Status Input 4-6
17R – Status Input 4-7
18L – Status Input 4-8
18R – Interlock Input 4